WHAT IS CLAIMED IS:

1. A multiprocessor system comprising:

a plurality of data processors, each data processor including:

a data processing core capable of data processing according to program control and memory access,

a memory forming a local portion of a unified memory shared among said plurality of data processors, and

a global memory arbitration logic connected to said data processing core and said memory of each of said data processors, said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor and a far connection to said data processing core of additional data processors, said global memory arbitration logic arbitrating access to said close portion of said unified memory granting a first type access to close data processing cores and a second type access different from aid first type access to far data processing cores.

2. The multiprocessor system of claim 1, wherein:

said local portion of said unified memory of each data processor is a dual port memory having a first port and a second port; and

said global memory arbitration logic arbitrating access to said first port of said dual port memory among said close data processing cores thereby providing said first type access

and arbitrating access to said second port of said dual port memory among said far data processing cores thereby providing said second type access.

3. The multiprocessor system of claim 2, wherein:

said first port of said dual port memory provides access to said dual port memory during a first portion of a repetitive time cycle; and

said second port of said dual port memory provides access to said dual port memory during a second portion of said repetitive time cycle different from said first portion of said repetitive time cycle.

4. The multiprocessor system of claim 2, wherein:

each of said data processors further includes a peripheral bus connected to said dual port memory for read and write access; and

said global memory arbitration logic grants read access requests on said peripheral bus highest priority access to said first port and grants write access request on said peripheral bus highest priority access to said second port.

5. The multiprocessor system of claim 2, wherein:

each of said data processors further includes a local memory connected to said data processing core and directly accessible by said data processing core and not directly accessible by data processing cores of other data processors.

6. A multiprocessor system comprising:

a plurality of data processors, each data processor including:

a data processing core capable of data processing according to program control and memory access,

a memory forming a local portion of a unified memory shared among said plurality of data processors having a first port and a second port, and

a global memory arbitration logic connected to said data processing core and said memory of each of said data processors, said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor and a far connection to said data processing core of additional data processors, said global memory arbitration logic arbitrating access to said first port of said dual port memory among said close data processing cores thereby providing a first type access and arbitrating access to a second port of said dual port memory of another data processor among said data processing cores having a far connection to said global memory arbitration logic of said another data processor thereby providing a second type access.

7. The multiprocessor system of claim 6, wherein:

said first port of said dual port memory provides access to said dual port memory during a first portion of a repetitive time cycle; and

said second port of said dual port memory provides access to said dual port memory during a second portion of said repetitive time cycle different from said first portion of said repetitive time cycle.

8. The multiprocessor system of claim 6, wherein:

each of said data processors further includes a peripheral bus connected to said dual port memory for read and write access; and

said global memory arbitration logic grants read access requests on said peripheral bus highest priority access to said first port and grants write access request on said peripheral bus highest priority access to said second port.

9. The multiprocessor system of claim 6, wherein:

each of said data processors further includes a local memory connected to said data processing core and directly accessible by said data processing core and not directly accessible by data processing cores of other data processors.

10. The multiprocessor system of claim 6, wherein:

said plurality of data processors consists of four data processors;

said global memory arbitration logic of each data processor has a close connection to its corresponding data processor and another data processor and has a far connection to two other data processors.